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Architecture-independent programming and automatic parallelisation have long been regarded as two different means of alleviating the prohibitive costs of parallel software development. Building on recent advances in both areas, Architecture-Independent Loop Parallelisation proposes a unified approach to the parallelisation of scientific

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Architecture-independent programming and automatic parallelisation have long been regarded as two different means of alleviating the prohibitive costs of parallel software development.

[The Effectiveness of Architecture-Independent Loop ...](#)
In the previous chapters, we introduced a series of techniques for the architecture-independent parallelisation

of loop computations, and we described a scheduling tool that implements a subset of these techniques. In order to assess the effectiveness as well as the limitations of our approach, this

A Strategy and a Tool for Architecture-Independent Loop ...

Based on the two classes of parallelisation techniques described so far, this chapter proposes a novel, two-phase strategy for the parallelisation of sequential loop nests.

This strategy attempts to apply template-matching scheduling in its former phase, and uses generic loop nest scheduling as a

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An instruction set architecture is distinguished from a microarchitecture, which is the set of processor design techniques used, in a particular processor, to implement the instruction set.